What is claimed is:

1. In a field programmable Gate Array, a programmable input / output architecture comprising:
at least one fuse address driver,
at least one programmable voltage supply driver,
programmable input / output buffers,
means to program the input / output buffers to a desired configuration.

2. The input / output architecture of claim 1, where the programmable input / output buffers further include at least 2 programmable antifuse matrix cells.

3. The input / output architecture of claim 1, where each programmable input / output buffer includes a set of programmable antifuse matrix cells.

4. The input / output architecture of claim 3, where each set includes 16 programmable antifuse matrix cells.

5. The input / output architecture of claim 4, where each set is connected to 8 fuse address drivers and two programmable voltage supply drivers.

6. The input / output architecture of claim 1, where the programmable input / output buffer includes programmable antifuse matrix cells and a programmable input / output driver circuit.

7. The input / output architecture of claim 1, where said means to program includes programmable antifuse matrix cells.

8. The input / output architecture of claim 1, where said desired configuration includes a plurality of I/O standards.

9. A programmable antifuse matrix cell comprising:

A two terminal antifuse
An N-channel transistor
A p-channel transistor
One terminal of said antifuse connected to a first source / drain terminal of said N-channel transistor and to a first source / drain terminal of said P-channel transistor and to an output node
Second terminal of said antifuse connected to ground
The gates of two said transistors are connected
The second source / drain terminal of said N-channel transistor is connected to a first voltage
Second source / drain terminal of said P-channel transistor is connected to a second voltage

10. The programmable antifuse matrix cell of claim 9 where the gate of the N-channel transistor is connected to an input node and the gate of the P-channel transistor is connected to ground.

11. The programmable antifuse matrix cell of claim 9 where the output node further drives an inverter

12. A programmable input / output driver circuit comprising:
Two or more P-channel pullup transistors
Two or more N-channel pulldown transistors
Each pullup or pulldown transistor is driven by a logic gate
Separate configuration signals driving each of above logic gates
Two or more input buffer types
A multiplexor connected to said input buffers
Configuration signals driving select input of said multiplexor

13. The programmable input / output driver circuit of claim 12 where said configuration signals are generated by programmable antifuse matrix cells.

14. The programmable input / output driver circuit of claim 12 where said input buffer types are input standards

15. The programmable input/output driver circuit of claim 12 where configuration signals can configure it to implement a plurality of I/O standards.